APPEAL BRIEF

1. Real Party in Interest

The real party in interest for this application is the assignee:

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An assignment has been recorded for this United States Patent Application.

2. Related Appeals and Interferences

There are no related appeals or interferences for this United States Patent application.

3. Status of the Claims

Claims 1-20 remain in this application. No claims have been allowed.

4. Status of the Amendments

An Amendment, dated 09 April 2001, was submitted after a first office action, mailed 12 January 2001. This Amendment was entered. No Amendment was made to the claims after the office action made FINAL mailed on 23 October 2001.

5. Summary of Invention

The invention is a method for forming a damascene multi-level conductor interconnection layer with improved properties upon a substrate employed within a microelectronics fabrication.

CLAIM 1 IS READ ON THE SPECIFICATION AND DRAWINGS AS FOLLOWS:

1.A method for forming a patterned microelectronics layer, comprising:

providing a substrate having a contact region formed thereon; (THIS COMPLETES FIG. 1; SEE DESCRIPTION ON PAGE 8)

forming over the substrate a first lower sub-layer and a second upper sub-layer to provide a composite etch stop layer;

forming over the composite etch stop layer an inter-level metal dielectric (IMD) layer;

forming over the IMD layer a photoresist mask layer pattern of an interconnection line trench pattern centered over the contact layer (THIS COMPLETES FIG. 2; SEE DESCRIPTION ON PAGE 9) and transferring the pattern by etching while employing a first etching method through the IMD layer and the second upper sub-layer of the composite etch stop layer to the first lower sub-layer of the composite etch stop layer;(THIS COMPLETES FIGURE 3; SEE DESCRIPTION ON PAGE 10) and etching while employing a second etch method the first lower sub-layer from the trench pattern for the interconnection lines.(THIS COMPLETES FIGURE 4; SEE DESCRIPTION ON PAGE 12)

CLAIM 12 IS READ ON THE SPECIFICATION AND DRAWINGS AS FOLLOWS:

12. A method for forming a patterned microelectronics layer comprising:

providing a substrate having a contact region of tungsten metal formed thereon; (THIS COMPLETES FIG 6; SEE DESCRIPTION ON PAGES)

forming over the substrate a first lower organic polymer sub-layer and a second upper sub-layer to provide a composite etch stop layer;

forming over the composite etch stop layer a blanket inter-level metal dielectric (IMD) layer;

forming over the blanket IMD layer a photoresist mask layer pattern of an interconnection line trench pattern centered over the contact region (THIS

COMPLETES FIGURE 7; SEE DESCRIPTION ON PAGE) and transferring the pattern while employing a first etch method through the blanket IMD layer and the second upper sub-layer of the composite etch stop layer to the first lower organic polymer sub-layer of the composite etch stop layer (THIS COMPLETES FIGURE 8; SEE DESCRIPTION ON PAGE); and

stripping the photoresist mask pattern and simultaneously etching the first lower organic polymer sub-layer to complete the formation of the interconnection trench pattern centered over the tungsten metal stud contact region.(THIS COMPLETES FIGURE 9; SEE DESCRIPTION ON PAGE).

Dependent claims 2-11 and 13-20 describe added important and critical/unexpected details based on experimental results to the independent claims.

6. Issues

Whether or not claims 1-7 and 9-11 are unpatentable over Zhao et al. in view of Hsiao Whether or not claim 8 is unpatentable over Zhao et al. in view of Hsiao and further in view of Sliwa et al.. Whether or not claims 12-20 are unpatentable over Zhao et al. in view of Hsiao and further in view of Cronin et al.

7. Grouping of Claims

Claims 1-11 and 12-20 are in a single group of claims.

8. ARGUMENT

Reconsideration of the rejection of Claims 1-7 and 9-11 under 35 U.S.C 103 over Zhao et al. in view of Hsiao. of the Examiner is respectfully requested for the following reasons.

Applicants' invention is a method for forming a patterned damascene multi-level conductor interconnection layer upon a substrate employed within a microelectronics fabrication. The conductor layer pattern is inlaid within an inter-level metal dielectric (IMD) layer by selective etching of a composite etch stop layer composed of two sub-layers through a photoresist etch mask layer.

It is agreed that Zhao et al. do not teach the method of applicants' invention in each and every limitation; in fact, the method employed by Zhao requires the employment of two or more additional dielectric layers than does the applicants' invention to accomplish the formation of the inlaid pattern. This is stated in Claim 1 of Zhao's teaching. Applicants' invention does not require these additional layers, and employs a composite etch stop layer instead. ✓

Reconsideration of the rejection of Claim 8 under 35 U.S.C. 103 over Zhao et al. in view of Hsiao and further in view of Sliwa et al. of the EXAMINER is respectfully requested for the following reasons.

Applicants' invention claims the employment of a silicon oxynitride layer deposited employing plasma enhanced chemical vapor deposition. The specific employment of this layer as a aprt of the composite etch stop layer is a key element of applicants' invention. Although the deposition of silicon containing layers by means of various chemical vapor deposition methods is taught by the references cited, trhe specific application, method and employment as cited in the applicants' invention is not found specifically in the references.

Reconsideration of the rejection of calims 12-20 under 35 U.S.C. 103 over Zhao et al. in view of Hsiao and further in viewe of Cronin et al. opf the EXAMINER is respectfully requested for the following reasons.

The teachings of Zhao.lead to the employment of at least two more dielectric layers over the method described by applicants' base claim 12. Further, the method of

applicants' invention combines the employment of an organic polymer dielectric sub-layer with another dielectric sub-layer to provide a composite etch stop layer. This permits the simultaneous removal of the orgainc polymer sub-layer with that of the photoresist etch mask layer. This key feature is not taught singly or in combination by Zhao, Hsiao or Cronin.

Applicants request that the Board of Appeals reverse the holding of the Examiner in finally rejecting the Claims in the application. Allowance of all claims is requested.

Respectfully submitted,

Stephen B. Ackerman (Reg. No. 37,761)

ADDENDUM

The claims outstanding in this application for United States Patent are as follows:

1. A method for forming a patterned microelectronics layer comprising:

providing a substrate having a contact region formed therein;

forming over the substrate a first lower sub-layer and a second upper sub-layer to provide a composite etch stop layer;

forming over the composite etch stop layer an inter-level metal dielectric (IMD) layer;

forming over the IMD layer a photoresist mask layer pattern of an interconnection line trench pattern centered over the contact layer and transferring the pattern by etching while employing a first etching method through the IMD layer and the second upper sub-layer of the composite etch stop layer to the first lower sub-layer of the composite etch stop layer;

etching while employing a second etch method the first lower sub-layer from the trench pattern for the interconnection lines.

2. The method of Claim 1 wherein by employing the first lower sub-layer there is avoided etching of the contact region within the first etching method.

3. The method of Claim 1 wherein the first lower sub-layer has a higher etch rate in the second etching method than the contact region;

4. The method of Claim 1 wherein forming a damascene multi-layer conductor interconnection layer is accomplished by the method further comprising:

forming a barrier metal layer over the patterned substrate; and

filling the trench pattern with a conductor material to complete the damascene multi-layer conductor interconnection layer structure.

5. The method of Claim 1 wherein the microelectronics layer is selected from the group consisting of:

microelectronics conductor layers;

microelectronics semiconductor layers;

microelectronics dielectric layers.

6. The method of Claim 1 wherein the substrate is a substrate employed within a microelectronics fabrication selected from the group consisting of:

integrated circuit microelectronics fabrications;

charge coupled device microelectronics fabrications;

solar cell microelectronics fabrications;

light-emitting diode microelectronics fabrications;

ceramic substrate microelectronics fabrications; and

flat panel display microelectronics fabrications.

7. The method of Claim 1 wherein the first lower sub-layer is formed employing a silicon oxide dielectric material formed employing plasma enhanced chemical vapor deposition (PECVD).

8. The method of Claim 1 wherein the upper second sub-layer is formed employing a silicon oxynitride dielectric material deposited employing plasma enhanced chemical vapor deposition (PECVD).

9. The method of Claim 1 wherein the contact region via conductor stud layer material is formed employing tungsten metal.

10. The method of Claim 1 wherein the inter-level metal dielectric (IMD) layer is formed employing silicon oxide dielectric material employing chemical vapor deposition (CVD).

11. The method of Claim 4 wherein the said conductor material is copper metal.

12. A method for forming a patterned microelectronics layer comprising:

providing a substrate having a contact region of tungsten metal conductor studs formed therein;

forming over the substrate a first lower organic polymer sub-layer and a second upper sub-layer to provide a composite etch stop layer;

forming over the composite etch stop layer a blanket inter-level metal dielectric (IMD) layer;

forming over the blanket IMD layer a photoresist mask layer pattern of an interconnection line trench pattern centered over the contact region and transferring the pattern while employing a first etch method through the blanket IMD layer and the second upper sub-layer of the composite etch stop layer to the first lower organic polymer sub-layer of the composite etch stop layer; and

stripping the photoresist mask pattern layer and simultaneously etching the first lower organic polymer sub-layer to complete the formation of the interconnection trench pattern centered over the tungsten metal stud contact region.

13. The method of Claim 12 wherein by employing the first lower organic polymer sub-layer there is avoided the etching of the tungsten metal stud contact region within the first etch method.

14.. The method of Claim 12 wherein forming a damascene multi-layer conductor interconnection layer structure is accomplished by the method further comprising:

forming a barrier metal layer over the substrate; and

filling the interconnection trench pattern with a conductor material to complete the damascene multi-level conductor interconnection layer structure.

15. The method of Claim 12 wherein the semiconductor substrate is a silicon semiconductor substrate.

16. The method of Claim 12 wherein the first lower organic polymer sub-layer is formed employing a low dielectric constant spin-on-polymer (SOP) dielectric material.

17. The method of Claim 12 wherein the second upper sub-layer is formed employing chemical vapor deposition (CVD) of silicon containing dielectric material.

18. The method of Claim 12 wherein the inter-level metal dielectric (IMD) layer is formed of silicon oxide dielectric material employing chemical vapor deposition (CVD).

19. The method of Claim 14 wherein the conductor material employed to fill the interconnection trench is copper.

20. The method of Claim 14 wherein the barrier metal layer is formed employing tantalum nitride (TaN).

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